PTO/SB/08A (08-03)

Substitute for form 1449A/PTO		Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*		Application Number	09/828,600
		Filing Date	April 6, 2001
		First Named Inventor	Uht, Augustus K.
		Art Unit	2183
		Examiner Name	Richard L. Ellis
Sheet	1 of 8	Attorney Docket Number	022193-010210US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number — Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document — Country Code[3]	Number[4]	Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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NON PATENT LITERATURE DOCUMENTS

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Examiner Signature	*Richard Ellis*	Date Considered	7/13/2005

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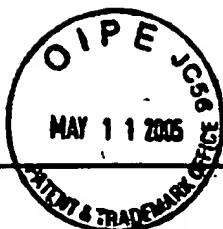
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	Filing Date	April 6, 2001
	First Named Inventor	Uht, Augustus K.
	Art Unit	2183
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(init)	47	Lilja, "Reducing the Branch Penalty in Pipelined Processors," *COMPUTER*, vol. 21, pp. 47-55, July 1988.	
(init)	48	Lipasti et al., "Superspeculative Microarchitecture for Beyond AD 2000," *IEEE COMPUTER*, vol. 30, no. 9, pp. 59-66, September 1997.	
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(init)	50	Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors," in *Proceedings of the 22nd Annual International Symposium on Computer Architecture*, pp. 138-149, IEEE and ACM, May 1995.	
(init)	51	Martin et al., "Timestamp snooping: An approach for extending smps," in *Proceedings of the International Conference on Architectural Suport for Programming Languages and Operating Systems*, pp. 25-36, November 2000.	
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(init)	53	Morano et al., "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," in *Proceedings of the Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy Related Issues (MEDEA 2 002)*, at PACT 2002. Charlottesville, Virginia, USA, September 22, 2002, pp 16-25. Also appears in ACM SIGARCH Computer Architecture Newsletter, March 2003, URL: http://www.ele.uri.edu/~uht/papers/MEDEA2002final.pdf.	
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(init)	59	Park et al., "Reducing Register Ports for Higher Speed and Lower Energy," in *Proceedings of the 35th Annual International Symposium on Microarchitecture*. Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
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RUE	61	Popescu et al., "The Metaflow Architecture," *IEEE MICRO*, vol. 11, no. 3, June 1991, pp. 10-13 & 63-73.	
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RLE	92	Uht, "High Performance Memory System for High ILP Microarchitectures," Technical Report 0797-0002, Department of Electrical and Computer Engineering, University, of Rhode Island, August 26, 1997. Available via http://ele.uri.edu/~uht, 10 pages total.	
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